PRODUCT

Embedded Line Controller

Manufacturing Embedded Line Controller And Xilinx Zynq

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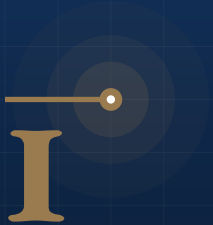

Introduction

MANUFACTURING EMBEDDED LINE CONTROLLER AMD XILINX ZYNQ

Introduction

Our client is a factory-equipment builder. Their product is an embedded line controller — the board that holds a factory line to its takt time. They were mid-development — rev A boards driving test rigs, a design freeze scheduled — when we collaborated with them on this project by providing independent verification and validation of the board. The design is a standalone AMD Xilinx Zynq-7000: one Cortex-A9 core runs Linux and the application plane, the second A9 is dedicated as the companion real-time processor, and the FPGA fabric provides deterministic I/O timing that neither core is asked to guarantee.

Introduction

- Compute topology: a single Zynq-7000 package — Cortex-A9 core 0 for Linux and the application, core 1 dedicated bare-metal as the internal real-time companion, and fabric blocks generating deterministic I/O timing.
- Under validation: a PROFINET port and an EtherCAT port on separate PHYs, thirty-two opto-isolated 24 V digital inputs, sixteen opto-isolated high-side outputs, four analog 4–20 mA input channels, two incremental encoder inputs into the fabric, RS-485, DDR3, QSPI boot flash, SD storage, and the 24 V industrial power entry with surge protection.
- Program state: mid-development — rev A functional on test rigs, one layout iteration before freeze.

Introduction

- Independence: no technical, managerial, or financial stake in the design; the builder's factory customers demand evidence their line's controller was proven by someone other than its designer.
- Bounded scope: independent validation only — no PLC-logic development, no firmware authoring, no out-of-scope engineering.
- Working inputs: the hardware design package — schematics, ICDs, BOM — with no access to firmware source.

2

Hardware Topology

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Hardware Topology

Topologically this is a standalone SoC with the companion role assigned to the second on-die core: an asymmetric multiprocessing split where core 1 and the fabric together fill the role a discrete real-time microcontroller would on other designs. Scope enclosed the board, its field interfaces, and its panel environment; the machine-control application and factory acceptance testing stayed outside.

- Topology classification: standalone Zynq-7000 in AMP configuration — Linux on core 0, bare-metal real-time executive on core 1, communicating through OCM shared memory with software interrupts, fabric I/O blocks owned by core 1.

Hardware Topology

- The companion core's job: the 500 µs I/O scan, encoder capture from the fabric, EtherCAT cyclic processing, output interlocks, and the watchdog over the Linux side.
- In-scope interfaces: PROFINET, EtherCAT, RS-485, DI x32, DO x16, AI x4 (4–20 mA), encoder x2, DDR3, QSPI, SD, and the 24 V entry with its surge stage.
- Envelope in scope: 0 °C to +60 °C panel interior, 24 V rails per industrial practice including contactor and drive transients, continuous three-shift duty.
- Out of scope: machine-control logic, factory acceptance, CE machinery-directive assessment — we produce integration evidence; the builder's assessor and factory customers judge it.

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Hardware Topology

- The Zynq family is one of the six architectures Polaris already runs on, so the OS baseline was inherited and effort went to this board's delta rather than silicon bring-up.

3

Problem Statement

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Problem Statement

Rev A ran the lab rig well, one layout iteration remained, and the application team was scaling up — while the board's behavior in an electrically hostile panel, under years of three-shift duty, existed only as extrapolation. A line controller that resets stops a line, and a stopped line is billed in cost per minute.

- Proven in isolation, never as a board: the Zynq, PHYs, opto-couplers, and analog front ends each carried vendor data — none of it with this board's isolation partitioning, its DDR3 routing, its fabric-timed output stages, or its 24 V entry sharing a panel with contactors and VFDs.

Problem Statement

- Firmware coverage is feature-shaped, not board-shaped: the application exercised PROFINET, most DIs, and half the DOs, but the EtherCAT port (a roadmap feature), eight DO channels, the second encoder input, and the analog channels' fault behavior fell outside every sprint.
- No stress, no extremes, no duration: no 60 °C panel soak under full I/O load, no multi-week three-shift endurance, no contactor-transient and surge campaign at the 24 V entry, no DDR3 margining at temperature.
- Nothing runs alongside development: validation was an end-gate, so an electrical-immunity defect would surface on a customer's factory floor as an unexplained line stop — billed, by contract, as downtime.

Problem Statement

- The builder's factory customers require documented controller evidence in their acceptance packages; the machinery-safety assessor expects characterized behavior under electrical fault.
- The fabric-timed outputs claimed 1 μs determinism — a claim that is a property of this board's clocking and needed measurement, not assertion.
- One layout iteration remained: every fault found after freeze becomes a firmware workaround or a field liability.

4

Customer Requirements

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Customer Requirements

The client's requirements were direct: validate the whole board, under stated limits, before the freeze, with evidence fit for factory acceptance packages.

- Operating temperature: the board shall operate from 0 °C to +60 °C panel interior.
- Supply voltage: 24 V DC nominal industrial supply, operating window 20.4 V to 28.8 V (24 V ±20%). The board shall survive contactor-class transients and surges per IEC 61000-4-5 at the 24 V entry without reset or damage; over-voltage protection shall clamp above 30 V continuous.

Customer Requirements

- Brown-out: the board shall ride through input sag to 18 V for 10 ms without reset; below that it shall shut down cleanly with no record loss and outputs driven to their defined safe state.
- Over-current: each of the sixteen high-side outputs shall have per-channel over-current protection tripping at 0.7 A within 10 ms with per-channel diagnostics; a shorted output shall not disturb any other channel.
- Determinism: fabric-timed outputs shall hold 1 µs determinism at the 500 µs scan.
- Humidity: the board shall operate at up to 90% RH non-condensing and shall not be exposed beyond that.

Customer Requirements

- Full-board functional validation: both A9 cores in their AMP roles, the fabric I/O blocks, DDR3, QSPI, SD, both fieldbus ports, all thirty-two DIs and sixteen DOs, all four analog channels, both encoders, and RS-485 — one integrated system.
- Coverage independent of firmware scope: every subsystem validated regardless of the application roadmap, through a HAL built from the design package.
- Stress matrix: 0–60 °C panel sweep, three-week three-shift endurance at full I/O load, contactor-transient and surge campaigns at the 24 V entry, DDR3 margining across temperature, fieldbus timing under saturation, and determinism measurement of the fabric outputs — vibration per panel-mount profile.

Customer Requirements

- Continuous validation alongside development: CI integration revalidating every firmware candidate on rev A, then the frozen layout.
- Evidence: timestamped, operator-attributed, version-pinned records with bidirectional traceability, packaged for factory acceptance and the machinery-safety file.
- A web console the builder's test technicians run without embedded expertise.
- An immutable, append-only evidence store anchoring the freeze decision and production baselines.
- Setup in minutes: documented bench — board, I/O load fixtures, fieldbus partners, programmable 24 V source, host — reproducible by any technician.

Architecture

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Architecture

The controller runs the validation OS, HAL, and client; an external x86 host runs the server, dashboard, and SDK. Execution stays isolated from data processing and the board keeps its resources for representative behavior — decisive here because the determinism claims under test would be destroyed by heavy on-target tooling.

- Polaris OS (the validation OS) — a reproducible Linux image for core 0 booting to a known state, with the AMP partition to core 1 loaded deterministically — one baseline across the rev A set.

Architecture

- HAL — the single board-specific layer, exercising the fabric I/O blocks, both fieldbus ports, all I/O banks, analog channels, encoders, DDR3, and storage behind a uniform interface that keeps the manufacturing suites portable to the frozen layout.
- Client — the on-target agent driving tests through the HAL; gRPC on the Linux core, FlatBuffers to the bare-metal companion core's executive; three timestamps per event (origin, relay, server); light enough that the 500 µs scan under measurement stays clean.
- Server — orchestration, scheduling, and the append-only records store on the host, four boards in parallel, dashboard and API hosted.

Architecture

- Dashboard — the technician console: provision a board, configure and launch, live scan-time histograms, I/O state matrices, fieldbus health, rail telemetry, time-series review; every state-changing action operator-attributed.
- Python SDK — automation and CI; scripts everything the console does; C bindings served the transient-injection sequencer.
- The OS and HAL are the two board-specific layers and were heavily modified for this board and this SoC; the client, server, dashboard, and Python SDK were configured to the client's requirements, but their core structure and working style remain the same across every board and every industry.

6

Design

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Design

The binding constraints: a 500 µs scan with 1 µs output determinism, a 60 °C panel beside switching contactors, an AMP architecture with no hardware lockstep to lean on, and factory customers who read acceptance evidence critically.

- Validation OS design — read-only rootfs, A/B partitions with rollback, and a boot chain that loads core 1's executive before Linux claims the interconnect, because the reverse order let Linux briefly own fabric clocks the companion core depended on; the trade-off is a slower Linux boot, accepted. The companion core runs a bare-metal executive rather than an RTOS — trading scheduling convenience for a provable worst case.

Design

- HAL design — partitioned by schematic sheet against ICD clauses; fabric events, encoder edges, and fieldbus cyclic data are interrupt-driven while analog channels and rail telemetry poll on the scan. OCM contention was the known risk: HAL calls from Linux touching shared memory during core 1's scan window measurably jittered it, so the interface was rebuilt around double-buffered exchange with scan-boundary handoff.
- Client design — origin timestamps latched in fabric registers for I/O events, correlated to the Linux clock at each scan boundary; on 24 V events the client flushes raw records first, so every transient leaves a complete record.

Design

- Server design — three-timestamp causality orders a contactor transient against the scan overrun it caused; retention sized for three-week endurance from four boards, with per-scan histograms aggregated hourly after campaign windows close.
- Dashboard design — scan-time histograms, output-determinism spreads, per-bank I/O matrices, fieldbus error counters, and rail telemetry are first-class views — the triage order of a controls test technician; run health and drop counts on every screen.
- SDK design — the client scripted the acceptance gate, the transient matrix, and the determinism sweeps; the direct API path served single-bank bench checks, at the stated cost that those runs produce no records.

Design

- OS and HAL design was board-specific and heavily reworked; the four upper components were configured to this builder’s workflow while their structure and working style stayed constant.

7

Implementation

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Implementation

Work went to the OS delta, the HAL, and the manufacturing campaigns; the four upper components were configured, not constructed.

- Validation OS — Yocto image for the Zynq-7000: inherited boot chain (FSBL, U-Boot) with the AMP load sequence corrected, board device tree covering PHYs, I/O banks, and analog front ends, minimal kernel; OTA with A/B rollback; boot under 30 seconds including bitstream and core 1 executive; per-build SBOM with CVE tracking; the companion-core executive built in the same tree.

Implementation

- HAL — implemented sheet by sheet and bench-verified as written: register interfaces to the fabric I/O and encoder blocks, double-buffered OCM exchange, PHY management for both fieldbus ports, opto-bank drivers with per-channel diagnostics, 4–20 mA channel drivers with open-loop detection; the design-package pass surfaced a schematic-to-BOM mismatch — DDR3 termination called for 39 Ω resistors on the schematic while the BOM listed 47 Ω, a margin loss confirmed later in temperature sweeps and corrected at the freeze.
- Client — C++ daemon on core 0, event and polling paths, fabric-correlated timestamping, transient-hardened flushing, gRPC upstream, FlatBuffers to core 1.

Implementation

- Server — telemetry receiver, versioned schema, scheduler, REST API, dashboard hosting, four-board parallelism.
- Dashboard — board provisioning, campaign configuration, live scan and I/O streaming, time-series review, export for acceptance packages, operator attribution.
- SDK — Python bindings, C transient-sequencer bindings, example scripts, CI wiring firing the acceptance suite on every firmware candidate.
- Board-specific: OS delta and HAL. Configuration: client correlation, server retention, dashboard views, SDK sequencer glue.

8

Test - IV&V

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Test - IV&V

Testing ran stack-first, then OS/HAL, then the board across one-shot, long-running, event-based, and monitoring campaigns — every dashboard-launched run committed to the append-only store.

- Stack self-verification: 100% test coverage of the client, server, dashboard, and Python SDK before it produced evidence about this controller.
- OS/HAL verification: A/B boot and rollback exercised, OTA verified end to end including the bitstream and core 1 executive, boot integrity checked on accept and reject paths.

Test - IV&V

- Bench setup: board cabled to I/O load fixtures, PROFINET and EtherCAT partner devices, encoder simulators, and a programmable 24 V source with transient generator, provisioning from the dashboard — documented, under thirty minutes.
- Functional campaign: PROFINET exchange suites, EtherCAT cyclic and mailbox suites, per-channel DI/DO verification with diagnostics, analog accuracy and open-loop detection, encoder count-integrity at rated frequencies, RS-485 margin, fabric output-determinism measurement.

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Test - IV&V

- Watchdog and reset campaign: the companion core's watchdog over Linux exercised with induced core 0 hangs — all sixteen outputs verified to hold their defined safe state through detection, reset, and AMP reload — plus warm/cold reset combinations confirming the corrected boot order holds under every restart path, not just clean power-on.
- Debug posture: JTAG access verified disabled in the production configuration — a panel-mounted controller on a factory network should not expose a debug port — with full debug retained on rev A boards for fabric-level trace during determinism measurement.
- One-shot tests as the acceptance gate: one pass/fail per subsystem per firmware candidate.

Test - IV&V

- Long-running: the three-week three-shift endurance at full I/O load caught DDR3 correctable-error onset above 55 °C — the termination BOM finding made measurable — and a slow drift in analog channel 3's offset traced to an opto-coupler LED aging out of family, flagged to procurement.
- Event-based: silent runs recording on scan overruns, I/O state anomalies, fieldbus errors, and rail events — this mode caught the main defect: a contactor-class transient at the 24 V entry reset the board outright, traced to the surge stage's MOV clamping voltage sitting above the downstream regulator's absolute maximum, a design error corrected at the freeze with a properly coordinated protection ladder.

Test - IV&V

- Monitoring: passive telemetry — rails, panel-simulated temperature, scan statistics, fieldbus counters — through transient campaigns; determinism measurement showed fabric outputs holding 0.4 µs spread while Linux-requested outputs through the OCM path spread to 180 µs under load — both numbers now documented facts rather than claims.
- Instrumentation correlation: oscilloscope and transient-generator captures anchored the reset defect, the protection-ladder coordination, and the determinism spreads to the records.

Test - IV&V

- Recording rule: every run launched from the dashboard is recorded, always, into the append-only store; the Python SDK can run 100% of what the dashboard can run — module, peripheral, or system level — for quick independent checks, and SDK-launched runs of this kind are not written to the records store. The store is the evidence; the SDK is the bench tool.
- Traceability: requirements traced bidirectionally to tests and records, schemas version-pinned, runs reproducible for factory acceptance.

9

Deliverables

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Deliverables

The builder received the complete platform fitted to this controller — source, records, procedures, no lock-in.

- Validation OS image with the full Yocto build system, AMP boot recipes, and per-build SBOM.
- Board-specific BSP and HAL source for every subsystem, maintained against the design package through the freeze.
- Compiled client for core 0 plus the companion-core executive build.

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Deliverables

- Server and dashboard as deployment-ready containers on the builder's bench host.
- Complete suites — fieldbus, I/O, analog, encoder, determinism, thermal, endurance, transient — with recorded rev A baselines for the frozen layout's comparison.
- Python SDK with documentation, example scripts, transient-sequencer bindings, and CI integration gating every firmware candidate.
- The append-only records store as client property — the evidence base for factory acceptance packages.

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Deliverables

- The independent validation report: the transient-reset design error, the DDR3 termination mismatch, the determinism measurements, the analog-drift procurement flag, metrics, pass/fail, coverage.
- Bench procedures for acceptance and re-runs; full documentation; no lock-in.

Conclusion

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Conclusion

The design froze with its protection ladder properly coordinated, its DDR3 terminated as designed rather than as purchased, and its determinism claims converted from datasheet arithmetic into measured spreads — the difference between a controller that survives a panel and one that reboots with every contactor.

- The transient reset was the line-stopper: every contactor cycle in a customer's panel would have dropped the controller, billed as downtime under the builder's own contracts; it cost a protection-ladder redesign at the freeze instead of field retrofits across an installed base.

Conclusion

- The suites gate every firmware drop in CI and carry to the frozen layout with only the HAL delta re-verified. We produce the evidence — the builder's assessor and factory customers judge it.

Lessons Learned

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Lessons Learned

The engagement sharpened our treatment of AMP architectures and industrial electrical immunity.

- Protection-ladder coordination is now verified analytically from the BOM before the first transient is ever injected — the MOV-versus-regulator mismatch was findable on paper in an afternoon, and the bench merely confirmed it; DDR3 termination and every other margin-critical value likewise gets schematic-to-BOM cross-check during document review, where two of this board's defects lived.

Lessons Learned

- AMP without hardware separation demands explicit interconnect discipline: OCM contention between Linux and the companion core jittered the scan until the exchange was double-buffered, and the boot order that let Linux touch fabric clocks first was a latent race — on every future AMP engagement the core-to-core resource contract is validated as its own campaign before any timing claim is measured.

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LET'S TALK

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